EE/CprE/SE 492 Status Report 4
Feb 27– March 12

Group number: **22**

Project title: **ReRAM Compute ASIC Fabrication**

Client &/Advisor: **Cheng Wang & Henry Duwe**

Team Members/Role:

Ali Mannan
Tyler Kloser
Austin Miller
Vinicius Malaman Soares

- **Weekly Summary**
  - This week we made a good amount of progress on the fundamental modules for our characterizations and crossbar design.
  - We met with a member from the December 2024 ReRAM team (Jason Xie) to discuss some of the problems we've been running into and some things we should continue to look out for moving forward. We were able to figure out getting the ReRAM module to pass LVS, which is a huge milestone for us and means we are now ready to complete a 1-bit design.
- **Past week accomplishments**
  - Vinicius Malaman Soares: Tested TIA on my system. Looked into the need of a priority encoder. Started the design of a 2-bit Flash ADC.
  - Tyler Kloser: Nearly completed testing the inverter through precheck, had some delay due to freezing but has been solved. Brought an analog mux into schematic.
  - Ali Mannan: TIA module completed. Post-layout parasitics extracted. TIA works as expected when accounting for parasitic resistances and capacitances. Works well as a comparator also. Brainstormed ReRAM issues in weekly meeting.
  - Austin Miller: Reram passing LVS, some progress on caravel pre-check. Script progress. Got some good tips and insight into previous problems from Jason
- **Pending issues**
  - Tyler Kloser: N/A
  - Ali Mannan: Sheet resistances on PDK website do not match those in the design PDK used in XSchem. Using PDK as it appears in XSchem, simulates correctly.
  - Austin Miller: Caravel pre-check not passing with bare harness (LVS, Documentation).
  - Vinicius Malaman Soares: Finish 2-bit ADC.

- **Individual contributions**

NAME	Individual Contributions	Hours this period	HOURS cumulative
Tyler Kloser	Inverter precheck and analog mux	6	25
Ali Mannan	TIA Completed, Parasitics extracted and confirmed working as TIA and Comparator	12	45
Austin Miller	Reram LVS passing, unified script development, more cli learning	12	48
Vinicius Malaman Soares	Tested TIA design on my system. Priority encoder research. Started 2-bit ADC design	7	30

- **Comments and extended discussion**
    - N/A

Plans for the upcoming week

- Ali Mannan: Finish a 1-bit design up to layout, with all components. DAC (inverter) -> 1T1R -> TIA -> ADC (inverter)
- Tyler Kloser: Finish up the inverter precheck, test analog mux with simulations, maybe take other components through precheck
- Austin Miller: Complete 1T1R (hopefully min size and large sized) and bring through precheck
- Vinicius Malaman Soares: Finish 2-bit ADC and start on 4-bit ADC.

- **Summary of weekly advisor meeting**
    - This week we discussed finally passing LVS with reram and what that looks like moving forward. We also discussed what we covered with Jason to get everyone up to speed. Going forward, we are going to start putting together the progress we've made towards the final deliverable and what absolutely needs to be completed to have a successful project.